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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/688,975	10/21/2003	Yoichi Tamaki	HITA.0445 4204		
38327	7590 11/30/2005	EXAMINER			
REED SMI		DO, THUAN V			
	TEW PARK DRIVE, SU JRCH, VA 22042	ART UNIT	PAPER NUMBER		
			2825		
			DATE MAILED: 11/30/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	ı No.	Applicant(s)						
Office Action Summary		10/688,975	;	TAMAKI ET AL.	On					
		Examiner		Art Unit						
		Thuan Do		2825						
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply										
A SHOWHIC - Exter after - If NO - Failu Any r	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DATES as ions of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. Period for reply is specified above, the maximum statutory period we to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THI 36(a). In no even will apply and will , cause the applic	S COMMUNICATION t, however, may a reply be tim expire SIX (6) MONTHS from to become ABANDONED	I. lely filed the mailing date of this comm (35 U.S.C. § 133).						
Status										
2a)□	Responsive to communication(s) filed on <u>21 Oct</u> This action is FINAL . 2b)⊠ This Since this application is in condition for allowar closed in accordance with the practice under <i>E</i>	action is no	n-final. or formal matters, pro		erits is					
Dispositi	on of Claims									
5)□ 6)⊠ 7)□ 8)□ Applicati 9)□	Claim(s) 1-8 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw Claim(s) is/are allowed. Claim(s) 1-8 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or on Papers The specification is objected to by the Examine The drawing(s) filed on 21 October 2003 is/are: Applicant may not request that any objection to the or Replacement drawing sheet(s) including the correction.	r election red er. : a)⊠ accel drawing(s) be	quirement. oted or b)⊡ objected held in abeyance. See	e 37 CFR 1.85(a).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.										
Priority u	ınder 35 U.S.C. § 119									
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 6662344. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 										
2) Notice Notice Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date 10/21/2003		4) Interview Summary (Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:		52)					

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DETAILED ACTION

1. This office action is responsive to application filed on 10/21/2003. Claims 1-8 are pending in this office action.

Claim objections

Claim 1, the term "element isolation grooves reaching the isolation layer"; and Claim 3, the terms "the plurality of the first bipolar transistors function as a singular bipolar transistor" including "the singular bipolar transistor"; and are unclear to what applicants intend to mean. Clarification or correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being unpatentable over Uchida et al., Pat. No. 5214302.

Regarding claim 1: Uchida teaches a method comprising:

a silicon-on-insulator substrate including a base substrate, an insulating layer over the base substrate, and a semiconductor layer over the insulating layer (col. 1, lines 45-67 and figure 2);

electric circuit formed over the silicon-on-insulator substrate (Figure 2);

a plurality of semiconductor islands used as element-forming regions in a first area of the silicon-on-insulator substrate (Figure 2); and

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a plurality of first bipolar transistors formed in the respective semiconductor islands, and having respective an emitter region, a base region, and a collector region formed in the semiconductor layer (col. 4, lines 46-67);

wherein the plurality of semiconductor islands are isolated each other by element isolation grooves reaching the isolation layer of the silicon-on-insulator substrate (col. 20, lines 1-22); and

the emitter regions, the base regions, and the collector regions of the plurality of the first bipolar transistors are electrically connected by interconnection wirings respectively (col. 19, line 45 through col. 20, line 22).

Regarding claim 2: Uchida teaches a method with island (col. 3, lines 3-10).

Regarding claim 3: Uchida teaches a method with connections (col. 1, lines 45-62).

The remaining claims of 102(b) section contain features similar to the rejection of claims 1-3 and rejected in the rationale.

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being unpatentable over Uchida et al., Pat. No. 4746963.

Regarding claim 1: Uchida teaches a method comprising:

a silicon-on-insulator substrate including a base substrate, an insulating layer over the base substrate, and a semiconductor layer over the insulating layer (col. 1, lines 26-50);

electric circuit formed over the silicon-on-insulator substrate (col. 1, lines 26-50);

a plurality of semiconductor islands used as element-forming regions in a first area of the silicon-on-insulator substrate (col. 1, lines 26-50); and

a plurality of first bipolar transistors formed in the respective semiconductor islands, and having respective an emitter region, a base region, and a collector region

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formed in the semiconductor layer (col. 2, lines 52-67);

wherein the plurality of semiconductor islands are isolated each other by element isolation grooves reaching the isolation layer of the silicon-on-insulator substrate (col. 2, lines 52-67); and

the emitter regions, the base regions, and the collector regions of the plurality of the first bipolar transistors are electrically connected by interconnection wirings respectively (col. 1, lines 36-50).

The remaining claims of 102(b) section contain features similar to the rejection of claim 1 and rejected in the rationale.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 571-272-1891. The examiner can normally be reached on Monday-Friday 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone numbers for proceeding this application is 571 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do Primary examiner

11/27/2005